Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A programmable interface comprising:

a register file having a plurality of registers, each register having a type;

a run control register;

a microcontroller configured to bidirectionally communicate with the register file and the run control register;

a Code Store SRAM configured to bidirectionally communicate with the microcontroller; and

executable code, loaded onto the Code Store SRAM;

wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor; and

wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.

2. (Previously Presented) A device, as defined in claim 1, wherein the types of the registers are selected from a group that includes timer, General purpose, external I/O, internal I/O, shared, and interrupt.

3. (Previously Presented) A device, as defined in claim 2, wherein when one of the registers has a type of external I/O, the register including edge detect logic.

4. (Original) A device, as defined in claim 2, wherein the register type further includes FIFO registers, operative to communicate with a direct memory access controller.

5. (Previously Presented) A device, as defined in claim 3, wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page

synchronization interface.

6. (Original) A device, as defined in claim 1, wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM.

7. (Previously Presented) A device, as defined in claim 1, wherein the system processor is configured to bidirectionally communicate with the register file.